- the time limitation of the control operation of the micro-processor, improved by the use of the logical control (not DSP), see SDD and Figure 8;

- improved data transfer from data acquisition subsystems to DSP to empty FIFO memory for the next operation, realized by the use of a fast DSP-FIFO interface (Figure 1).

Using the system and method of the present invention, properties of the flow can be measured accurately even when the flow is highly non-uniform. Dual-plane EIT has the added advantage of providing on-line volume fraction and velocity distributions which can be used for the purposes of process monitoring and control.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention will now be more particularly described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 illustrates the system architecture;

Figure 2 shows one possible system configuration of a high performance two-phase flow meter using the DSP module as a building block, (a) Single Read-Operation Timing, (b) Single Write-Operation Timing;

Figure 3 illustrates the architecture of the EIT data acquisition subsystems (DAS);

Figure 4 shows a simplified schematic (a) and an equivalent schematic (b) for AD844;

Figure 5 shows a voltage controlled current source (VCCS);

Figure 6 shows the structure of the Equal-Width Pulse Synthesizer (EWPS);

Figure 7 shows waveforms generated by the EWPS;

Figure 8 shows the structure of the Synchronised Digital Demodulation (SDD);

Figure 9 shows the configuration of the sampling modes, (a) 4 samplings, (b) 8 samplings, (c) 16 samplings, (d) rolling-sample method;

Figure 10 shows an AC-coupling network;

Figure 11 shows the trigger circuit of the over zero switch (OZS);

Figure 12 shows a typical curve of independent measurements obtained from a phantom filled with mains tap water;

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Figure 13(a) shows photographs of two balls dropping, one relatively heavy and one relatively light;